ABSTRACT OF THE DISCLOSURE

A method and apparatus for analog-to-digital pipeline conversion are described. The apparatus includes a sample/hold circuit having an input to receive an analog input voltage, a comparator device coupled to the input of the sample/hold circuit to receive the analog input voltage, and a separate gain circuit coupled to an output of the sample/hold circuit and to the comparator device. The sample/hold circuit and the comparator device sample the analog input voltage and the separate gain circuit amplifies an analog residue voltage obtained from the analog input voltage to obtain an amplified analog residue voltage in a first phase of a non-overlapping clock. The analog residue voltage is obtained in a second phase of the non-overlapping clock, when the sample/hold circuit holds the analog input voltage sampled in the first phase, and the comparator device compares the analog input voltage sampled in the first phase with a reference voltage value.